ABSTRACT

Disclosed is a method of improving the immunity to interference of an integrated circuit (16) having error signals transferred between a microprocessor chip or multiple processor μC (1) and an additional component (2). For the transfer, a minimum pulse length that is independent of the clock frequency of the microprocessor or the microprocessors is defined, starting from which a signal on an error line having a defined pulse length is interpreted as an error. Also disclosed is an integrated circuit, which is designed so that the above method is implemented. The circuit has a microprocessor chip or multiple processor microcontroller (1) or microprocessor module and an additional component (2) having separately arranged power elements. The circuit also has pulse extending devices and/or signal delaying devices for the output of error pulses (6, 6') one after the other through at least one error line (3, 4).